IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
PATENT APPLICATION

Applicant: Mitchell DeMond, et al.. Art Unit:

Serial No.: 10/063,427 Examiner:

Filed: 04/23/02 Atty. Docket: BUR920010192US1

Title: PHYSICAL DESIGN CHARACTERIZATION SYSTEM

INFORMATION DISCLOSURE STATEMENT
UNDER 37 CFR 1.56, 1.97, 1.98

Honorable Commissioner of Patents and Trademarks
Washington, D. C. 20231

Sir:

Applicants submit herewith form PTO-1449, listing patents, publications, or other information of which they are aware which they believe may be material to patentability pursuant to 37 CFR 1.56(b), and in respect of which there may be a duty to disclose under 37 CFR 1.56(a), together with legible copies of the patents, publications, or other information listed.

While the items submitted with this Information Disclosure Statement may be material to patentability pursuant to 37 CFR 1.56, in accordance with 37 CFR 1.97(h) it shall not be construed to be an admission that any patent, publication, or other information cited is "prior art" or is material to patentability for this invention unless specifically designated as such. In accordance with 37 CFR 1.97(g), the filing of this Information Disclosure Statement shall not be construed to mean that a search has been made or that no other information material to patentability, as defined in 37 CFR 1.56(b), exists.

Respectfully submitted,

Date: 5/24/02 By: _____

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INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
BUR920010192US1	10/063427
Applicant(s) Mitchell DeHond, et al.	
Filing Date 04/23/02	**Group Art Unit**

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
		3,751,647	08/07/73	Maeder, et al.			
		5,084,824	01/28/92	Lam, et al.			
		5,438,527	08/01/95	Feldbaumer, et al.			
		5,539,652	07/23/96	Tegethoff			
		5,754,826	05/19/98	Gamal, et al.			
		5,773,315	06/30/98	Jarvis			
		5,953,518	09/14/99	Sugasawara, et al.			
		6,044,208	03/28/00	Papadopoulou, et al.			
		6,070,004	05/30/00	Prein			
		6,169,960	01/02/01	Ehrichs			
		6,210,983	04/03/01	Atchison, et al.			

FOREIGN PATENT DOCUMENTS

	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO
		JP6216249	08/05/94	Japan				
		JP1024225	09/11/98	Japan				

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

		Michael Retersdorf, "Yield Focused Defect Reduction Methodology", 3/99, IEEE/SEMI Advanced Semiconductor Manufacturing Conference, pp. 309 - 313
		K.W. Lallier and A.D. Savkar, "Relating Logic Design to Physical Geometry in LSI Chip", IBM Technical Disclosure Bulletin, Vol. 19 No. 6, November 1976, pp. 2140-2143.

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

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APPLICANT(S) Mitchell DeHond, et al.	
FILING DATE 04/23/02	GROUP

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
		6,305,004	10/16/01	Tellez, et al.			
		6,311,139	10/30/01	Kuroda, et al.			

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

			C.H. Stapper, "High Yield Semiconductor Logic Wiring", Vol. 30 No. 11 April 1988, IBM Technical Disclosure Bulletin, pp. 366-367.
			D.Guedj and M. Rivier, "Method to Computer the Random Photo Yield of Integrated Circuits", Vol. 32, No. 7, December 1989, IBM Technical Disclosure Bulletin, pp. 242 - 244.

EXAMINER	DATE C NSIDERED

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